What is claimed is:

1. A semiconductor integrated circuit device comprising:

a MISFET, having a source electrode and a drain electrode of a first conductivity type and a gate electrode, formed in a well of a second conductivity type; and

a body biasing circuit that generates a voltage in said well by passing a prescribed current in a forward direction into a diode formed from said well and said source electrode of said MISFET.

2. The semiconductor integrated circuit device as claimed in claim 1, wherein:

said semiconductor integrated circuit device comprises a plurality of circuit blocks; and

said body biasing circuit is provided for each of said circuit blocks.

3. The semiconductor integrated circuit device as claimed in claim 2, further comprising a power control unit which controls said body biasing circuit individually for each corresponding one of said circuit blocks.

4. The semiconductor integrated circuit device as claimed in claim 2, a power control soft ware module is carried out on a CPU, and controls said body biasing circuit individually for each corresponding one of said circuit blocks.

5. The semiconductor integrated circuit device as claimed in claim 4, wherein said each circuit block comprises a register, and said each body biasing circuit is controlled in accordance with data stored in said register.

6. The semiconductor integrated circuit device as claimed in claim 5, wherein said each circuit block is connected to a data bus, the data of said resister being written through said data bus.

7. The semiconductor integrated circuit device as

claimed in claim 1, wherein:

said semiconductor integrated circuit device comprises a plurality of circuit blocks; and

said body biasing circuit is provided for each of said circuit blocks, and is controlled by a control signal generated for a corresponding one of said circuit blocks.

8. The semiconductor integrated circuit device as claimed in claim 1, wherein:

said semiconductor integrated circuit device comprises a plurality of circuit blocks;

said circuit block includes a plurality of functional blocks; and

said body biasing circuit is provided for each of said functional blocks.

9. The semiconductor integrated circuit device as claimed in claim 1, wherein:

said semiconductor integrated circuit device comprises a standard cell block; and

said body biasing circuit is provided for each row of said standard cell block.

10. The semiconductor integrated circuit device as claimed in claim 1, wherein said body biasing circuit includes a current source provided between a first power supply line and a contact region of said well, and passes said prescribed current into said diode via said contact region.

11. The semiconductor integrated circuit device as claimed in claim 10, wherein said current source generates said prescribed current using said first power supply line as a power supply source.

12. The semiconductor integrated circuit device as claimed in claim 11, wherein said current source comprises:

a current-source first MISFET having the same polarity as said MISFET, and whose gate electrode is supplied with a control signal and whose source electrode

is connected to a second power supply line;

a current-source second MISFET having a different polarity from said MISFET, and whose source electrode is connected to said first power supply line and whose drain electrode and gate electrode are connected to a drain electrode of said current-source first MISFET; and

a current-source third MISFET connected to said current-source second MISFET in a current-mirror configuration, and whose drain is connected to said contact region.

13. The semiconductor integrated circuit device as claimed in claim 12, wherein said current source further comprises:

a current-source fourth MISFET having the same polarity as said MISFET, and whose gate electrode is supplied with an inverted version of said control signal and whose source electrode is connected to said contact region and whose drain electrode is connected to said second power supply line.

14. The semiconductor integrated circuit device as claimed in claim 11, wherein said current source comprises:

a current-source fifth MISFET having a different polarity from said MISFET, and whose gate electrode is supplied with a control signal and whose source electrode is connected to said first power supply line; and

a current-source sixth MISFET having the same polarity as said MISFET, and whose gate electrode is supplied with said control signal and whose source electrode is connected to said contact region and whose drain electrode is connected to a second power supply line.

15. The semiconductor integrated circuit device as claimed in claim 1, wherein operation delay is made constant against temperature changes by operating said

semiconductor integrated circuit device with a low voltage at which said semiconductor integrated circuit device exhibits the characteristic that a leakage current increases and the delay decreases with increasing temperature.

16. A semiconductor integrated circuit device comprising:

a first MISFET of a first polarity, having a source electrode and a drain electrode of a first conductivity type and a gate electrode, formed in a first well of a second conductivity type;

a second MISFET of a second polarity, having a source electrode and drain electrode of said second conductivity type and a gate electrode, formed in a second well of said first conductivity type;

a first body biasing circuit that generates a voltage in said first well by passing a prescribed current in a forward direction into a diode formed from said first well and said source electrode of said first MISFET; and

a second body biasing circuit that generates a voltage in said second well by passing a prescribed current in a forward direction into a diode formed from said second well and said source electrode of said second MISFET.

17. The semiconductor integrated circuit device as claimed in claim 16, wherein:

said semiconductor integrated circuit device comprises a plurality of circuit blocks; and

said first and second body biasing circuits are provided for each of said circuit blocks.

18. The semiconductor integrated circuit device as claimed in claim 17, further comprising a power control unit which controls said first and second body biasing circuits individually for each corresponding one of said circuit blocks.

19. The semiconductor integrated circuit device as

claimed in claim 17, a power control soft ware module is carried out on a CPU, and controls said body biasing circuit individually for each corresponding one of said circuit blocks.

20. The semiconductor integrated circuit device as claimed in claim 19, wherein said each circuit block comprises a register, and said each body biasing circuit is controlled in accordance with data stored in said register.

21. The semiconductor integrated circuit device as claimed in claim 20, wherein said each circuit block is connected to a data bus, the data of said resister being written through said data bus.

22. The semiconductor integrated circuit device as claimed in claim 16, wherein:

said semiconductor integrated circuit device comprises a plurality of circuit blocks; and

said first and second body biasing circuits are provided for each of said circuit blocks, and are controlled by a control signal generated for a corresponding one of said circuit blocks.

23. The semiconductor integrated circuit device as claimed in claim 16, wherein:

said semiconductor integrated circuit device comprises a plurality of circuit blocks;

said circuit block includes a plurality of functional blocks; and

said first and second body biasing circuits are provided for each of said functional blocks.

24. The semiconductor integrated circuit device as claimed in claim 16, wherein:

said semiconductor integrated circuit device comprises a standard cell block, and

said first and second body biasing circuits are provided for each row of said standard cell block.

25. The semiconductor integrated circuit device as

claimed in claim 16, wherein:

said first body biasing circuit includes a first current source provided between a first power supply line and a contact region of said first well, and passes said prescribed current into said first diode via said contact region of said first well; and

said second body biasing circuit includes a second current source provided between a second power supply line and a contact region of said second well, and passes said prescribed current into said second diode via said contact region of said second well.

26. The semiconductor integrated circuit device as claimed in claim 25, wherein said first current source generates said prescribed current using said first power supply line as a power supply source, and said second current source generates said prescribed current using said second power supply line as a power supply source.

27. The semiconductor integrated circuit device as claimed in claim 26, wherein:

said first current source comprises:

a first-current-source first MISFET having the same polarity as said first MISFET, and whose gate electrode is supplied with a first control signal and whose source electrode is connected to said second power supply line;

a first-current-source second MISFET having a different polarity from said first MISFET, and whose source electrode is connected to said first power supply line and whose drain electrode and gate electrode are connected to a drain electrode of said first-current-source first MISFET; and

a first-current-source third MISFET connected to said first-current-source second MISFET in a current-mirror configuration, and whose drain is connected to said contact region of said first well, and

said second current source comprises:

a second-current-source first MISFET

having the same polarity as said second MISFET, and whose gate electrode is supplied with a second control signal and whose source electrode is connected to said first power supply line;

a second-current-source second MISFET having a different polarity from said second MISFET, and whose source electrode is connected to said second power supply line and whose drain electrode and gate electrode are connected to a drain electrode of said second-current-source first MISFET; and

a second-current-source third MISFET connected to said second-current-source second MISFET in a current-mirror configuration, and whose drain is connected to said contact region of said second well.

28. The semiconductor integrated circuit device as claimed in claim 27, wherein:

said first current source further comprises a first-current-source fourth MISFET having the same polarity as said first MISFET, and whose gate electrode is supplied with an inverted version of said first control signal and whose source electrode is connected to said contact region of said first well and whose drain electrode is connected to said second power supply line; and

said second current source further comprises a second-current-source fourth MISFET having the same polarity as said second MISFET, and whose gate electrode is supplied with an inverted version of said second control signal and whose source electrode is connected to said contact region of said second well and whose drain electrode is connected to said first power supply line.

29. The semiconductor integrated circuit device as claimed in claim 26, wherein:

said first current source comprises:

a first-current-source fifth MISFET having a different polarity from said first MISFET, and

whose gate electrode is supplied with a first control signal and whose source electrode is connected to said first power supply line; and

a first-current-source sixth MISFET having the same polarity as said first MISFET, and whose gate electrode is supplied with said first control signal and whose source electrode is connected to said contact region of said first well and whose drain electrode is connected to said second power supply line, and

said second current source comprises:

a second-current-source fifth MISFET having a different polarity from said second MISFET, and whose gate electrode is supplied with a second control signal and whose source electrode is connected to said second power supply line; and

a second-current-source sixth MISFET having the same polarity as said second MISFET, and whose gate electrode is supplied with said second control signal and whose source electrode is connected to said contact region of said second well and whose drain electrode is connected to said first power supply line.

30. The semiconductor integrated circuit device as claimed in claim 16, wherein operation delay is made constant against temperature changes by operating said semiconductor integrated circuit device with a low voltage at which said semiconductor integrated circuit device exhibits the characteristic that a leakage current increases and the delay decreases with increasing temperature.